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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,011	11/26/2003	Christoph Heer	INF 2002 P 10624 US	7561

48154 7590 10/09/2007

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EXAMINER	
COUGHLAN, PETER D	
ART UNIT	**PAPER NUMBER**
2129	

MAIL DATE	DELIVERY MODE
10/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/724,011	HEER, CHRISTOPH	
	Examiner	Art Unit	
	Peter Coughlan	2129	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

1. This office action is in response to an AMENDMENT entered October 17, 2007 for the patent application 10/724011 filed on November 26, 2003.

2. All previous office actions are fully incorporated into this Final Office Action by reference.

Status of Claims

3. Claims 1-14 are pending.

Objections

4. Applicant makes the statement 'In fact Rule 83(a) very specifically states that convention features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention, should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation.'

It seems the applicant did not comprehend the Examiner's concerns wherein the previous office action the Examiner cited numerous examples of problems with the only drawing within the specification in addition the Examiner cited a problem with the overall design of the circuit. The applicant's response with Rule 83(a) does not answer any of the Examiners questions of clarity regarding the diagram and the problems remain. Standard electronic circuits schematic notations is easily found and used worldwide. For example the two references, which the applicant supplied in the information disclosure statements, use standard schematic notation. The applicant's position to use their own notation without essential description is not acceptable.

Claims 1, 5, 6, 7, 10, 11, 14 are objected to based on all these claims pertain to the 'logic circuit' (item 8). Concerning Control Block (item 8). According to the diagram there are 6 inputs (none of which is a clock input, see below) and a single output. There is no diagram which illustrates the internal circuit which discloses the logic how the output (item 11) is reached. The diagram and specification are silent regarding the contents of item 8. This non-description reasoning of that output 11 is correct is not acceptable. There needs to be some diagram which discloses the internal workings of item 8.

These objections must be addressed and the indicated problem corrected.

Claims 1, 6, 9 are objected to the due to the input parameters of the multiplexer. Concerning connections between devices being unclear, the Examiner will restate the

objections. For example item 1 is input which consists of 1-n input values. These inputs go to comparator 6 (and 16) and also to multiplexer 3 (and 13) It is known within the art that multiplexers have 2 different inputs, but these are not labeled within the diagram. In addition the number of inputs for these two types of inputs do not have the same number of inputs. But according to the diagram there are the same number of inputs going to the comparator as to the multiplexer and there are the same number of inputs coming from the comparator as to the multiplexer. Thus the multiplexer is getting the same number of inputs from the input (item 1) and from the comparator (item 6) which can't happen at all. The statement within the specification, 'Simultaneously, these data are led in one part of the bit width of the input data bus 7 to the corresponding multiplexer control input of the first and/or second multiplexer 3' does not make sense and looking at the diagram, it makes no sense to do this function.

These objections must be addressed and the indicated problem corrected.

Claims 2, 3, 6, 9, 12, 13 are objected to based on the lack of description of the 'comparator circuit.' An additional problems are what type of 'comparator' is being used? Are they 'and' gates, 'or' gates, 'nor' gates or some combination of standard thereof? Worded another way, 'and', 'nand', 'or' or 'nor' gates each have their own corresponding truth table. What is the truth table for the 'comparator' circuit? Claim 12 does not specifically mention a 'comparator circuit' but does mention the 'means for comparing the comparison data.

These objections must be addressed and the indicated problem corrected:

Claim 12 is objected to based on the assumption of the ability to 'storing the comparison data.' An additional problem with the diagram is how do the registers get initialized with initial values so that they can be used in conjunction with the comparators? Per the specification ¶0006 these registers or 'look up tables' are composed of RAM. RAM needs to be initialized. There is no input to these registers or 'look up tables.'

This objection must be addressed and the indicated problem corrected.

Claims 4 and 8 are objected to based on lack of input and output parameters and associated connections of registers, comparators, multiplexers, and control logic circuits. A FPGA acts like a ASIC only with different performance properties and turn around time. A circuit is a circuit regardless of other characteristics. There exists a problem with the overall design of the invention as well. Per the specification the circuit realizes an 'if then else' branch.

A 'if then else' design has three main components, 'Statement A', 'result B' and 'result C.' It works by if 'Statement A' is true then 'result B' is outputted and if 'Statement A' is false then 'result C' is outputted. Therefore there are 3 registers needs to realize an 'if then else' branch. One for 'Statement A', 'result B' and 'result C'. The invention only has two registers. Also there is only one comparison ('Statement A'), but the invention has two comparators, which makes no sense. There needs to be only one multiplexer but the invention has two of them. The output of the comparator needs to

control the multiplexer, but in the invention the output of the comparators lead to a control logic in which nothing is described within the specification.

The Examiner cannot assume connections and possible functions for given items within the diagram and lack of explanation within the specification. With this in mind, the Examiner cannot see how the invention works.

These objections must be addressed and the indicated problem corrected.

35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-14 are rejected under 35 U.S.C. 101 for nonstatutory subject matter. The invention lacks utility. The invention as described within the specification and only diagram will not work as equivalent to an 'if-then-else' statement.

Concerning connections between devices being unclear, the Examiner will restate the objections. For example item 1 is input which consists of 1-n input values. These inputs go to comparator 6 (and 16) and also to multiplexer 3 (and 13) It is known

within the art that multiplexers have 2 different inputs, but these are not labeled within the diagram. In addition the number of inputs for these two types of inputs do not have the same number of inputs. But according to the diagram there are the same number of inputs going to the comparator as to the multiplexer and there are the same number of inputs coming from the comparator as to the multiplexer. Thus the multiplexer is getting the same number of inputs from the input (item 1) and from the comparator (item 6) which can't happen at all.

Concerning Control Block (item 8). According to the diagram there are 6 inputs (none of which is a clock input, see below) and a single output. There is no diagram which illustrates the internal circuit which discloses the logic how the output (item 11) is reached. The diagram and specification are silent regarding the contents of item 8. This non-description reasoning of that output 11 is correct is not acceptable. There needs to be some diagram which discloses the internal workings of item 8.

Concerning input 10 in which the applicant states that 'The specification never states that control input 10 is limited to a clock signal nor that the second input of the CLB control logic 8 is limited to a clock input.' The applicant is correct with this statement and the Examiner made this conclusion based on the fact that the triangle shape in item 8 is standard notation which represents a clock input. This is widely used for example, looking at the EP 0410759A2 (which is supplied by the applicant) which shows FF1 and FF2 with the triangle shape being connected to K Clock. Applicant now states on the record that there is no clock input on the invention.

An additional problems are what type of 'comparator' is being used? Are they 'and' gates, 'or' gates, 'nor' gates or some combination of standard thereof? Worded another way, 'and', 'nand', 'or' or 'nor' gates each have their own corresponding truth table. What is the truth table for the 'comparator' circuit?

Another additional problem with the diagram is how do the registers get initialized with initial values so that they can be used in conjunction with the comparators? Per the specification ¶0006 these registers or 'look up tables' are composed of RAM. RAM needs to be initialized. There is no input to these registers or 'look up tables.'

There exists a problem with the overall design of the invention as well. Per the specification the circuit realizes an 'if then else' branch.

A 'if then else' design has three main components, 'Statement A', 'result B' and 'result C.' It works by if 'Statement A' is true then 'result B' is outputted and if 'Statement A' is false then 'result C' is outputted. Therefore there are 3 registers needs to realize an 'if then else' branch. One for 'Statement A', 'result B' and 'result C'. The invention only has two registers. Also there is only one comparison ('Statement A'), but the invention has two comparators, which makes no sense. There needs to be only one multiplexer but the invention has two of them. The output of the comparator needs to control the multiplexer, but in the invention the output of the comparators lead to a control logic in which nothing is described within the specification.

The Examiner cannot assume connections and possible functions for given items within the diagram and lack of explanation within the specification. With this in mind,

the Examiner cannot see how the invention works. Resulting in lack of utility and the rejection of claims 1-14.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-14 are rejected under 35 USC 112, first paragraph because current case law (and accordingly, the MPEP) require such a rejection if a 101 rejection is given because when Applicant has not in fact disclosed the practical application for the invention, as a matter of law there is no way Applicant could have disclosed how to practice the undisclosed practical application. This is how the MPEP puts it:

> ("The how to use prong of section 112 incorporates as a matter of law the requirement of 35U.S.C. 101 that the specification disclose as a matter of fact a practical utility for the invention.... If the application fails as a matter of fact to satisfy 35 U.S.C. 101, then the application also fails as a matter of law to enable one of ordinary skill in the art to use the invention under 35 U.S.C. § 112."); In re Kirk, '376 F.2d 936, 942, 153 USIPQ 48, 53 (CCPA 1967) ("Necessarily, compliance with § 112 requires a description of how to use presently useful inventions, otherwise an applicant would anomalously be required to teach how to use a useless invention."). See, MPEP 21107.01 (IV), quoting In re Kirk.

Therefore, claims 1-14 are rejected on this basis.

Response to Arguments

5. Applicant's arguments filed on October 17, 2007 for claims 1-14 have been fully considered but are not persuasive.

6. In reference to the Applicant's argument:

REMARKS
Claims 1-14 are pending in the present application. Claims 1, 2, 3, 4 and 5 have been amended. No new matter has been added.

Drawing Objection
The drawing has been objected to under 37 C.F.R. § 1.84(o). A replacement drawing sheet is provided herewith. In this amendment, labels have been added to the registers 4, 14, comparators 6, 16, multiplexers 3, 13, and control logic block 8.

Each of the objections will now be addressed.

1. Standardized shapes of drawings. The Office Action objects to the drawings for not having standardized shapes for the registers, comparators, multiplexers and control blocks. Applicant is unaware of any PTO requirement regarding the shapes of elements in block diagrams. In fact, Rule 83(a) very specifically states that "conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention, should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation (e.g., a labeled rectangular box)." 37 C.F.R. § 1.83(a), emphasis added. In this case, Applicant has complied with the rule by providing a labeled rectangular box. See also, Hellestrand, Fig. 16, element 1609, cited by the Examiner and showing a multiplexer is a labeled rectangular box. That being said, if the Examiner will provide additional guidance as to the desired shape, Applicant will provide a replacement drawing sheet consistent with that guidance.

Examiner's response:

The drawings are objected to because all elements in the figures and flow-charts are required to be distinctly labeled with appropriate legend. 37 CFR 1.84 (o). Correction is required. For example there are three regions within a multiplexer. One of these regions is call the 'selector' (or 'controller'). Since the applicant refuses to follow standard circuit diagrams, and the explanation of ¶0024 does not go into detail concerning the selector (or controller), the Examiner cannot determine the function of the drawing from the drawing itself or the specification. Office Action stands.

7. In reference to the Applicant's argument:

2. Connections between devices are unclear. The Office Action states that it makes no sense that the input to the comparators is also connected to the multiplexers. Paragraph 24 of the specification is very clear on this question.

From the data input 1 of the CLB 9, the resulting data are led via the input data bus 7 to the corresponding bus input of the first or second LUT 2; 12 and thus to the corresponding first bus input of the first or second comparator 6; 16. Simultaneously, these data are led in one part of the bit width of the input data bus 7 to the corresponding multiplexer control input of the first and/or second multiplexer 3; 13 and also to the first input of the CLB control logic 8. From the control input 10 of the CLB 9, the control data are led over the control data bus 7 to the second input of the CLB control logic 8.

Examiner's response:

The clarity of the English is fine but the meaning of the English makes no sense. For example 'Simultaneously, these data are led in one part of the bit width of the input data bus 7 to the corresponding multiplexer control input of the first and/or second multiplexer 3' does not make sense and looking at the diagram, it makes no sense to do this function. Office Action stands.

8. In reference to the Applicant's argument:

3. Control block. The Office Action states that the control block (presumably CLB control logic 8) needs to be diagrammed in standardized form. Once again, Applicant is unaware of any standardized form for a control block but remains willing to modify the drawing upon receipt of guidance. The operation of the control logic block is clearly described in the specification and the specific implementation is a matter of design choice that would be clear to one of ordinary skill in the art.

Examiner's response:

There are 6 inputs into item 8, control logic block and a single output. How does the CLB generate the only output. The Examiner asked for an internal diagram for this structure. Office Action stands.

9. In reference to the Applicant's argument:

4. Input 10. Input 10 illustrates a control input for the control logic block 8. "From the control input 10 of the CLB 9, the control data are led over the control data bus 7 to the second input of the CLB control logic 8." Par. [0024]. The specification never states that control input 10 is limited to a clock signal nor that the second input of the CLB control logic 8 is limited to a clock input.

Examiner's response:

The triangle shape within item 8 in the diagram is the standard for a clock input. The applicant states that this input is not to be limited to a clock input. In fact the work 'clock' is not mentioned within the specification. Without this, the circuit must have all information stored at the same time in order for the invention to run. Office Action stands.

10. In reference to the Applicant's argument:

5. "The applicant desires a patent without detail of the invention is unacceptable." Applicant respectfully submits that the drawings meet each and every rule required by the Patent Office. One of ordinary skill in the art, reading the specification and drawings would understand the details of the invention.

Examiner's response:

With all of the problems in basic design, lack of detail and Objections presented, the Examiner disagrees with the applicant. Office Action stands.

11. In reference to the Applicant's argument:

Section 101 Rejection
Claims 1-14 have been rejected under 35 U.S.C. § 101 for nonstatutory subject matter. Section 101 provides that a patent may be obtained for "any new and useful process, machine, manufacture or composition of matter." Claim 1 is directed to an arrangement that includes an input data node, a CLB control logic circuit, a look-up table, an input data bus, a multiplexer, a control input node and a register data bus. These are all tangible, concrete things. Similarly, claim 6 is directed to a logic circuit that includes a register, a comparator, a multiplexer and a control block and claim 11 is directed to means for performing a switching function, means for selecting at least a portion of the comparison data; and a CLB control logic circuit. Once again, these are tangible things. The Office Action states that "[t]here is no real world practical purpose for such a hardware device stated with the application." Applicant strongly disagrees. The claimed invention provides a circuit that is useful, concrete and tangible.
The claimed invention is useful. For example, embodiments of the invention provide a solution to the problem of minimizing the use of area for configurable array blocks. Par. [0015]. As another example, one configuration shows its advantage in that for the implementation of more than one conditional branch in an LUT, an additional savings of

hardware resources is achieved by reducing the required CLBs. Par. [0021]. Further, the invention is concrete and tangible. The claimed circuit recites very specific circuit elements such as an input data node, a CLB control logic circuit, a look\- up table, an input data bus, a multiplexer, a control input node and a register data bus. These physical elements are repeatable, non-unpredictable, real world and non-abstract.

The Office Action then concludes that "[the claimed invention] is just a collection of circuits, which the applicant claims parallels a if-then-else branch." Applicant respectfully submits that if you remove the pejorative characterizations "just" and "applicant claims" the conclusion itself recites statutory subject matter. A collection of circuits that performs a task is patentable. To state otherwise is simply wrong. That is the law.

Examiner's response:

With the lack of utility from the invention based on previously mentioned

statements, the 35 U.S.C. §101 rejection stands. Office Action stands.

12. In reference to the Applicant's argument:

Section 112 Rejection
Claims 1-14 were rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

The Office Action states there is no need for a second comparator or a second multiplexer and there is not a need for the results of both multiplexers to go into the control box. First, Applicant notes that only claim 9 recites a second comparator and a second multiplexer and, therefore, this rejection clearly has no bearing on claims 1-8 and 10-14.

With respect to the questions raised in the Office Action, Applicant respectfully directs the Examiner's attention to Paragraph [0019], which states

This special configuration of the solution according to embodiments of the invention shows its advantage in that for the implementation of more than one conditional branch in an LUT, an additional savings of hardware resources is achieved by reducing the required CLBs. In addition, here it is favorably guaranteed that the comparison data, which are stored in the LUT and which are required for processing with the CLB

controller, are also simultaneously already available for further processing in typical multiplexers of a CLB. Therefore, additional hardware, which would otherwise be necessary, is likewise spared for each CLB that is used.

With respect to the rejection under the written description requirement, Applicant respectfully submits that the specification describes the claimed invention in sufficient detail that one skilled in the art will reasonably conclude that the inventor had possession of the claimed invention. As stated in the MPEP, it is now well accepted that a satisfactory description may be in the claims or any other portion of the originally filed specification. MPEP § 2163. Since the claims are substantially unchanged from the originally filed, there can be no doubt that the inventor had possession of the claimed invention.

Examiner's response:

The Examiner withdraws the rejection.

Examination Considerations

13. The claims and only the claims form the metes and bounds of the invention. "Office personnel are to give the claims their broadest reasonable interpretation in light of the supporting disclosure. *In re Morris*, 127 F.3d 1048, 1054-55, 44USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. *In re Prater*, 415 F.2d, 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969)" (MPEP p 2100-8, c 2, l 45-48; p 2100-9, c 1, l 1-4). The Examiner has the full latitude to interpret each claim in the broadest reasonable sense. Examiner will reference prior art using terminology familiar to one of ordinary skill in the art. Such an approach is broad in concept and can be either explicit or implicit in meaning.

14. Examiner's Notes are provided to assist the applicant to better understand the nature of the prior art, application of such prior art and, as appropriate, to further indicate other prior art that maybe applied in other office actions. Such comments are entirely consistent with the intent and sprit of compact prosecution. However, and unless otherwise stated, the Examiner's Notes are not prior art but link to prior art that one of ordinary skill in the art would find inherently appropriate.

15. Examiner's Opinion: Paragraphs 13 and 14 apply. The Examiner has full latitude to interpret each claim in the broadest reasonable sense.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

17. Claims 1-14 are rejected.

Correspondence Information

18. Any inquiry concerning this information or related to the subject disclosure should be directed to the Examiner Peter Coughlan, whose telephone number is (571) 272-5990. The Examiner can be reached on Monday through Friday from 7:15 a.m. to 3:45 p.m.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor David Vincent can be reached at (571) 272-3080. Any response to this office action should be mailed to:

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(571) 272-3150 (for formal communications intended for entry.)

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Peter Coughlan

9/25/2007

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